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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/646,923	08/25/2003	Hong-gie Hwang	1293.1884	1952	
21171 7:	590 06/20/2006		EXAM	EXAMINER	
STAAS & HALSEY LLP SUITE 700		FLORES RUIZ, DELMA R			
1201 NEW YORK AVENUE, N.W.			ART UNIT	PAPER NUMBER	
WASHINGTO	N, DC 20005		2828		

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)			
Office Asticus Commons	10/646,923	HWANG, HONG-GIE			
Office Action Summary	Examiner	Art Unit			
	Delma R. Flores Ruiz	2828			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet wit	h the correspondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period was preply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNIC 36(a). In no event, however, may a rewill apply and will expire SIX (6) MONT, cause the application to become ABA	ATION. ply be timely filed  HS from the mailing date of this communic ANDONED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on 27 M	arch 2006.				
·_ ·	action is non-final.				
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E					
Disposition of Claims					
4)⊠ Claim(s) <u>1 and 3-34</u> is/are pending in the applic	cation.				
4a) Of the above claim(s) is/are withdraw					
5)⊠ Claim(s) <u>18-34</u> is/are allowed.					
6)⊠ Claim(s) <u>1 and 3-9</u> is/are rejected.	•				
7)⊠ Claim(s) <u>11-17</u> is/are objected to.	·	•			
8) Claim(s) are subject to restriction and/or	election requirement.				
Application Papers					
9) The specification is objected to by the Examine	r.				
10) The drawing(s) filed on is/are: a) acce		v the Examiner.			
Applicant may not request that any objection to the		=			
Replacement drawing sheet(s) including the correcti	• • • •	, ,	21(d).		
11) The oath or declaration is objected to by the Ex	= :				
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:	priority under 35 U.S.C. §	119(a)-(d) or (f).			
<ol> <li>Certified copies of the priority documents</li> </ol>	s have been received.				
2. Certified copies of the priority documents have been received in Application No					
3. Copies of the certified copies of the priority documents have been received in this National Stage					
application from the International Bureau	(PCT Rule 17.2(a)).				
* See the attached detailed Office action for a list of	of the certified copies not re	eceived.			
httschment(e)					
Attachment(s) ) Notice of References Cited (PTO-892)	4) 🔲 Interview Su	mman/ (DTO 442)			
) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)	Mail Date			
I) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Info 6) Other:	ormal Patent Application (PTO-152)			
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### **DETAILED ACTION**

# **Priority**

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al (6,775,216) in view of VanHoudt (2002/0121094).

Regarding claims 1, figure 9A of Kelly discloses generating an error voltage (VMDC) between an output voltage (PDO) of a laser diode (70) sampled during an automatic power control period and a reference voltage (280), the output voltage being an effective output voltage within a predetermined range (set by the amplifier 306), processing the error voltage (302) into a compensated control voltage and applying it to a laser diode (70).

Kelly discloses the claimed invention except for proportional-integral processing. However, it is well know in the art to apply the proportional-integral processing as discloses by VanHoudt in (Paragraphs [0011, 0035 and 0036]). Therefore, it would have been obvious to a person having ordinary skill in the art to apply the well know proportional-integral processing as suggested by VanHoudt to the laser of Kelly, because it will could be use to process the error voltage and produce a corresponding PI signal see (Paragraph [0035-0036]) of VanHoudt.

Regarding claim 3, the compensated control voltage applied to the laser diode (70) is an effective control voltage within a predetermined range (set by the amplifier 288).

Regarding claims 4 and 8, Figures 6 - 9A of Kelly discloses setting an automatic power control (see Figure Character 7, Character 190) for the laser diode

(see Fig. 9 Character 70); converting (see Fig. 6 Character 176, Column 7, Lines 35 – 39) an output voltage (PDO) of the laser (70) from an analog from to a digital form (Column 7, Lines 35 – 39), generating an error voltage (VMDC) between an output voltage (PDO) of a laser diode (70) sampled during an automatic power control period and a reference voltage (280), the output voltage being an effective output voltage within a predetermined range (set by the amplifier 306), processing the error voltage (302) into a compensated control voltage and applying it to a laser diode (70).

Kelly discloses the claimed invention except for proportional-integral processing. However, it is well know in the art to apply the proportional-integral processing as discloses by VanHoudt in (Paragraphs [0011, 0035 and 0036]). Therefore, it would have been obvious to a person having ordinary skill in the art to apply the well know proportional-integral processing as suggested by VanHoudt to the laser of Kelly, because it will could be use to process the error voltage and produce a corresponding PI signal see (Paragraph [0035-0036]) of VanHoudt.

Regarding claim 7, figure 9A of Kelly discloses generating an error voltage (VWDC) between an output voltage of a laser diode sampled during an automatic power control period and a reference voltage, the output voltage being an effective output voltage within a predetermined range (set by the amplifier 306), and processing the error voltage to generate a compensated control voltage and applying the compensated control voltage to the laser diode (70).

Art Unit: 2828

Kelly discloses the claimed invention except for proportional-integral processing. However, it is well know in the art to apply the proportional-integral processing as discloses by VanHoudt in (Paragraphs [0011, 0035 and 0036]). Therefore, it would have been obvious to a person having ordinary skill in the art to apply the well know proportional-integral processing as suggested by VanHoudt to the laser of Kelly, because it will could be use to process the error voltage and produce a corresponding PI signal see (Paragraph [0035-0036]) of VanHoudt.

Regarding claim 9, figure 9A of Kelly discloses an error voltage generation unit generating an error voltage (VWDC) between an output voltage (362) of a laser diode sampled during an automatic power control period and a reference voltage (286), the output voltage being an effective output voltage within a predetermined range (set by the amplifier 306), and a control voltage generation unit (302) processing the error voltage to generate an effective control voltage. Kelly discloses the claimed invention except for proportional-integral processing. However, it is well know in the art to apply the proportional-integral processing as discloses by VanHoudt in (Paragraphs [0011, 0035 and 0036]). Therefore, it would have been obvious to a person having ordinary skill in the art to apply the well know proportional-integral processing as suggested by VanHoudt to the laser of Kelly, because it will could be use to process the error voltage and produce a corresponding PI signal and for improved laser output stability see (Paragraph [0035-0036]) of VanHoudt.

# Allowable Subject Matter

Claims 18 – 34 are allowed.

Claims 10-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### Response to Arguments

Applicant's arguments with respect to claims 1, 3 - 34 have been considered but are most in view of the new ground(s) of rejection.

#### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Delma R. Flores Ruiz whose telephone number is (571) 272-1940. The examiner can normally be reached on M - F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Min Sun Harvey can be reached on (571) -272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Delma R. Flores Ruiz
Examiner

Art Unit 2828

DRFR/MH June 09, 2006 Min Sun Harvey
Supervisor Patent Examiner
Art Unit 2828

Page 8